International Journal of Electrical and Electronics Research ISSN 2348-6988 (online)
Vol. 3, Issue 1, pp: (213-217), Month: January - March 2015, Available at: www.researchpublish.com

Enhanced Auto-Gated Flip-Flop Using Clock Gating Technique with Sleep Transistor

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***Abstract*: The demand for power-sensitive design has grown significantly in recent years due to tremendous growth in portable applications. Consequently, the need for power efficient design techniques has grown considerably. Several efficient design techniques have been proposed to reduce both dynamic as well as static power in state-of-the-art VLSI circuit applications. With the scaling of technology and the need for higher performance and more functionality, power dissipation is becoming a major bottleneck for microprocessor designs. Clock power is significant in high-performance processors. Clock gating is very useful for reducing the power consumed by digital systems. Three gating methods are known. The most popular is synthesis-based, data-driven method and auto-gated FFs (AGFF).This paper presents a novel method called Look-Ahead Clock Gating (LACG), which combines all the three. Along with technology scaling down and higher operating speeds of CMOS VLSI circuits, the leakage power is getting enhanced. The low leakage FFs are designed using sleep transistors and simulated in tanner design environment using 90 nm and 45n technology files.**

***Keywords:* Clock gating, Static power, Leakage power, Sleep transistors.**

I. INTRODUCTION

One of the major dynamic power consumers in computing and consumer electronics products is the system's clock signal, typically responsible for 30% to 70% of the total dynamic (switching) power consumption . Several techniques to reduce the dynamic power have been developed, of which clock gating is predominant. Ordinarily, when a logic unit is clocked, its underlying sequential elements receive the clock signal regardless of whether or not their data will toggle in the next cycle. With clock gating, the clock signals are ANDed with explicitly redefined enabling signals. Clock gating is employed at all levels: system architecture, block design, logic design gates. Synthesis-based clock gating is the most widely used method by EDA tools.

II. DATA DRIVEN CLOCK GATING

To address the above redundancy, a method called *Data-driven clock gating* was proposed for flip-flops (FFs).There, the clock signal driving a FF, is disabled (gated) when the FF's state is not subject to change in the next clock cycle[9]. In an attempt to reduce the overhead of the gating logic, several FFs are driven by the same clock signal, generated by ORing the enabling signals of the individual FFs .

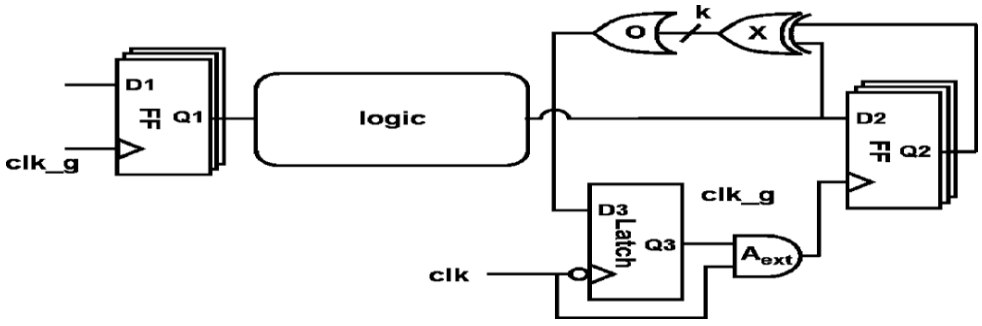

Fig: 1. Circuit implementation of data-driven clock gating

Data-driven gating suffers from a very short time-window. The cumulative delay of the XOR, OR, latch and the AND gater must not exceed the setup time of the FF.

III. AUTO-GATED FLIP-FLOPS

The basic circuit used for LACG is *Auto-Gated Flip-Flip*(AGFF) illustrated in Fig. 2.

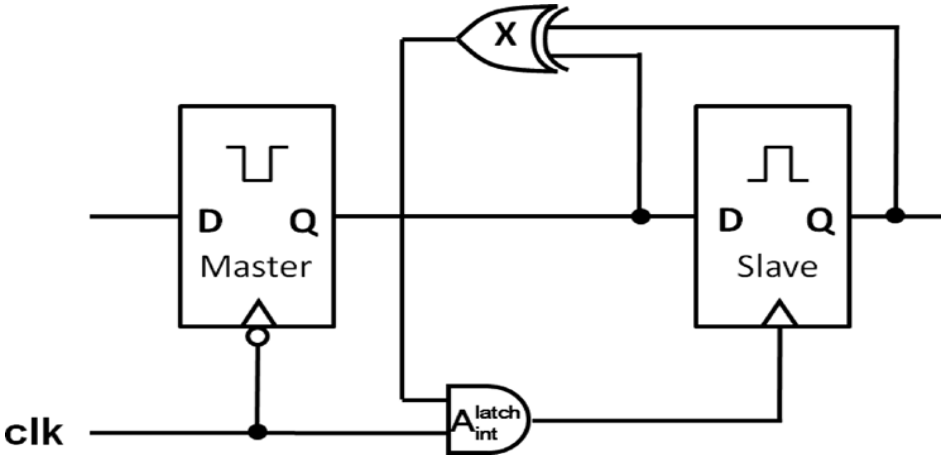

Fig: 3. An auto-gated flip-flop

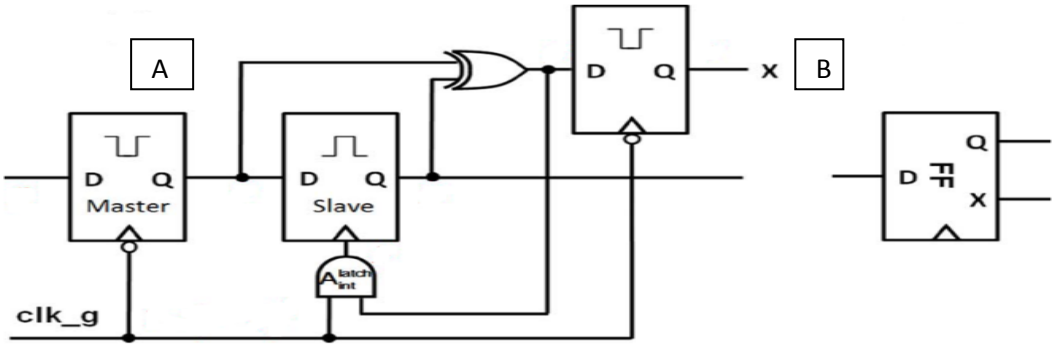

Fig: 4. Enhanced AGFF with XOR output used for LACG

The FF's master latch becomes transparent on the falling edge of the clock, when the master latch becomes opaque and the XOR gate indicates whether or not the slave latch should change its state.

IV. POWER DISSIPATION IN VLSI CIRCUITS

The total power dissipation in a circuit conventionally consists of two components, namely, the static and dynamic power dissipation.

Dynamic power:

For dynamic power dissipation there are two components one is switching power due to charging and discharging of load capacitance. The other is the short circuit power due to the nonzero rise and fall time of input waveforms. The switching power of a single gate can be expressed as

$$P_D = \alpha C_L V_{DD}^2 f$$

Where α is the switching activity,

f is the operation frequency,

C_L is the load capacitance,

V_{DD} is the supply voltage.

The short circuit power of an unloaded inverter can be approximately given by

$$P_{SC} = \beta (V_{DD} - V_{th})^{3} \tau / 12T$$

Where β is the transistor coefficient,

τ is the rise/fall time,

T (1/f) is the delay.

Leakage power

There are three dominant components of leakage in a MOSFET in the nanometer regime:

(1) Sub-threshold leakage, which is the leakage current from drain to source (I_{sub}).

(2) Direct tunneling gate leakage which is due to the tunneling of electron (or hole) from the bulk silicon through the gate oxide potential barrier into the gate.

(3) The source/substrate and drain/substrate reverse-biased p-n junction leakage.

V. CLOCK GATIG TECHNIQUE

Clock gating is an effective way of reducing the dynamic power dissipation in digital circuits. In a typical synchronous circuit such as the general purpose microprocessor, only a portion of the circuit is active at any given time. Hence, by shutting down the idle portion of the circuit, the unnecessary power consumption can be prevented. One of the ways to achieve this is by masking the clock that goes to the idle portion of the circuit. This prevents unnecessary switching of the inputs to the idle circuit block, reducing the dynamic power. The input to the combinational logic comes through the registers, which are usually composed of sequential elements, such as D flip-flops.

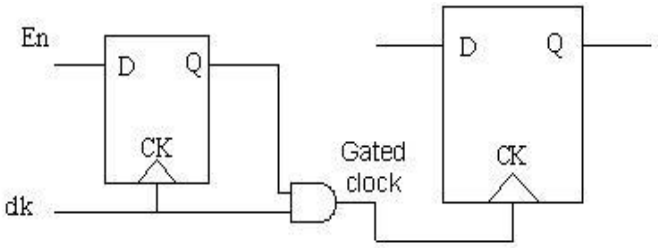

Fig: 5. Clock gating

Clock power is a major component of microprocessor power mainly because the clock is fed to most of the circuit blocks in the processor, and the clock switches every cycle. Thus the total clock power is a substantial component of total microprocessor power dissipation. Clock-gating is a well-known technique to reduce clock power. Because individual circuit usage varies within and across applications, not all the circuits are used all the time, giving rise to power reduction opportunity. By ANDing the clock with a gate-control signal, clock-gating essentially disables the clock to a circuit whenever the circuit is not used, avoiding power dissipation due to unnecessary charging and discharging of the unused circuits. Specifically, clock-gating targets the clock power consumed in pipeline latches and dynamic-CMOS-logic circuits (e.g., integer units, floating-point units, and word-line decoders of caches) used for speed and area advantages over static logic. Clock-gating schemes that either result in frequent toggling of the clock-gated circuit between enabled and disabled states, or apply clock-gating to such small blocks that the clock-gating control circuitry is almost as large as the blocks themselves, incur large overhead. This overhead may result in power dissipation to be higher than that without clock-gating.

VI. LOOK AHEAD CLOCK GATING

AGFF can also be used for general logic, but with two major drawbacks. Firstly, only the slave latches are gated, leaving half of the clock load not gated. Secondly, serious timing constraints are imposed on those FFs residing on critical paths, which avoid their gating. LACG takes AGFF a leap forward, addressing three goals; stopping the clock pulse also in the

master latch, making it applicable for large and general designs and avoiding the tight timing constraints. LACG is based on using the XOR output in Fig. 1 to generate clock enabling signals of other FFs in the system, whose data depend on that FF.

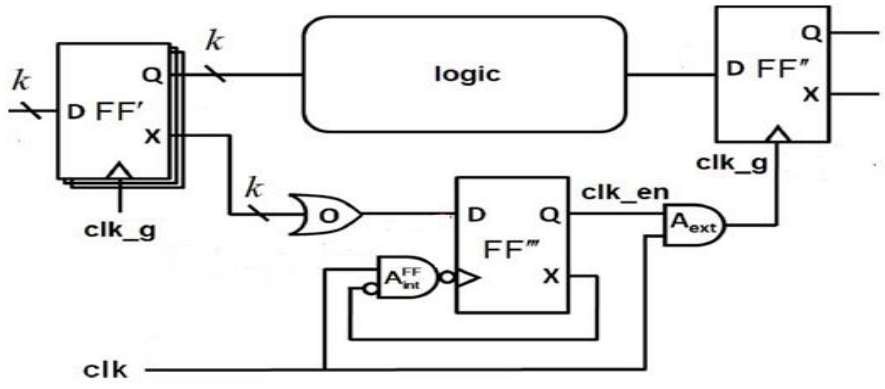

Fig: 6. LACG of general logic

VII. EXPERIMENTAL RESULTS

The gating scheme presented in Fig. 6 was first verified by a formal verification EDA tool and it was found equivalent to the original circuit before the gating logic was introduced. Though not surprising, it is a must in an industrial environment where the method was experimented. It is important to note that the introduction of LACG made most of the gate-level clock gating techniques employed by this design redundant. Those were therefore dropped, which somewhat compensated the LACG power and Area overhead.

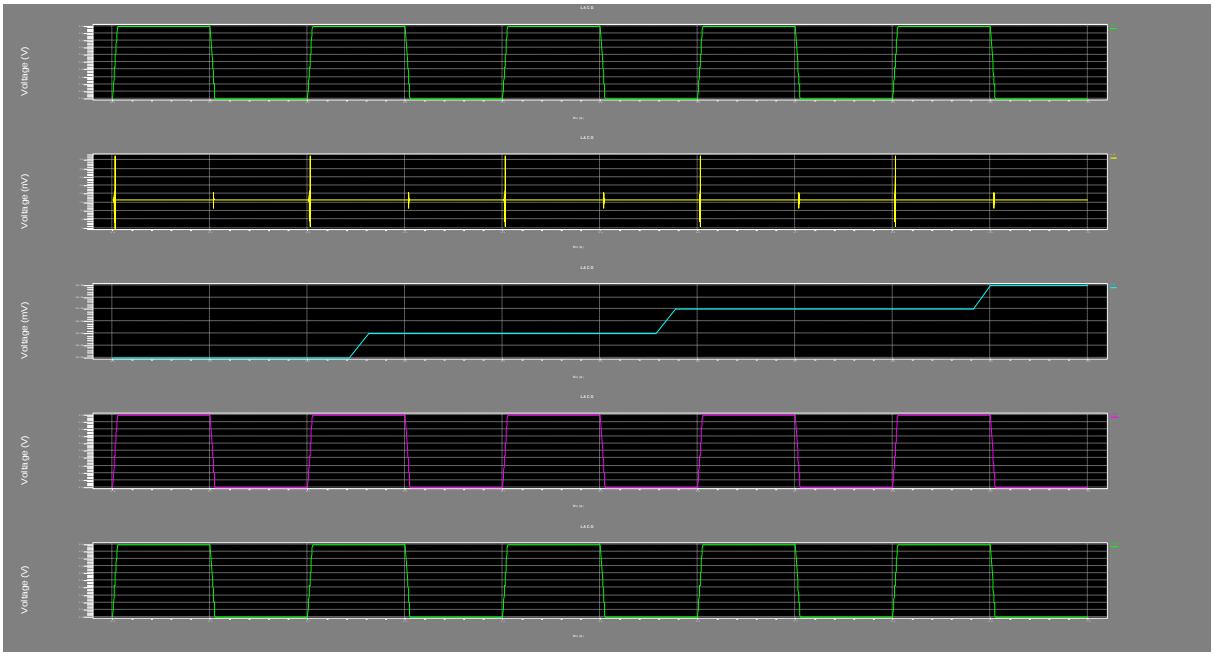

Fig.7 Wave form for LACG

VIII. CONCLUSION

The novel approach for save more power from the circuit that could be used as power gating technique. To reduce the standby mode leakage power this technique is very useful. The design could be done by 90nm and 45 nm technology and simulation could be done by TANNER T-SPICE technology. Further the leakage power has bend reduced by power gating technique. The parallel counter has been designed by using the auto gated flip flop design. The over all power has been reduced by this technique.

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